WHAT IS CLAIMED IS:

1. A method for manufacturing an active matrix liquid crystal device using five masks, comprising:

forming a plurality of gate electrodes over a substrate using a first mask;

forming a plurality of etch stoppers over the plurality of gate electrodes using a second mask, each etch stopper being formed over one gate electrode;

a plurality of drain electrodes and a plurality of source electrodes formed using a third mask, a portion of each of the drain electrodes being formed over a first portion of a corresponding one of the etch stoppers and a portion of each of the source electrodes being formed over a second portion of the corresponding one of the etch stoppers, wherein the source and the drain electrodes are separated over the corresponding one of the etch stoppers;

forming a passivation layer over the substrate having a plurality of via holes using a fourth mask; and

forming a pixel electrode over the passivation layer using a fifth mask.

2. The method of claim 1, further comprising:

forming a plurality of gate lines over the substrate using the first mask;

forming a gate insulating layer over the substrate and the plurality of gate lines, wherein the passivation layer is formed over the plurality of drain electrodes, the plurality of source electrodes and the gate insulating layer; and

etching at least one of the passivation layer and the gate insulating layer to form the plurality of via holes, the via holes exposing at least one of a portion of the plurality of drain electrodes, a portion of the plurality of source electrodes and a portion of the plurality of gate lines.

3. The method of claim 2, wherein an etching rate of the passivation layer is at least an etching rate of the gate insulating layer.

4. The method of claim 2, wherein the plurality of drain electrodes and the plurality of source electrodes are substantially unaffected by the etching step.

5. The method of claim 2, wherein the etching step applies a plasma taper-etch process having about 40 sccm of sulfur hexafluoride, about 32 sccm of oxygen and about 8 sccm of carbon tetrafluoride.

6. The method of claim 2, wherein the gate insulating layer is comprised of silicon nitride.

7. The method of claim 1, wherein the pixel electrode is comprised of indium-tin-oxide.

8. The method of claim 1, wherein the passivation layer is comprised of silicon oxynitride formed at a temperature of about 200°C.

9. An active matrix liquid crystal device, comprising:

a plurality of gate electrodes formed over a substrate and a plurality of gate lines formed over the substrate using a first mask;

a plurality of etch stoppers formed over the plurality of gate electrodes using a second mask, each gate stopper formed over one electrode;

a gate insulating layer formed over the substrate and the plurality of gate lines;

a plurality of drain electrodes and a plurality of source electrodes formed using a third mask, a portion of each of the drain electrodes being formed over a first portion of a corresponding one of the etch stoppers and a portion of each of the source electrodes being formed over a second portion of the corresponding one of the etch stoppers, wherein the source and the drain electrodes are separated over the corresponding one of the etch stoppers;

a passivation layer formed over the substrate, wherein the passivation layer is formed over the plurality of drain electrodes, the plurality of source electrodes and the gate insulating layer; and

a plurality of via holes ~~etched~~ through at least one of the passivation layer and the gate insulating layer exposing at least one of a portion of the plurality of drain electrodes, a portion of the plurality of source electrodes and a portion of the plurality of gate lines.

10. The active liquid crystal device of claim 9, wherein a first portion of the plurality of via holes is formed through the passivation layer and a second portion of the via hole is formed through the gate insulating layer, a value of an angle formed by a sidewall of the second portion of the plurality of via holes and a surface of the substrate being at least a value of an angle formed by a sidewall of the first portion of the plurality of via holes and the surface of the substrate.

11. The active liquid crystal device of claim ~~9~~ 10, wherein a distance between the sidewall of the first portion of the via hole and a via hole center is at least a distance between the sidewall of the second portion of the via hole and the via hole center.

12. The active matrix liquid crystal device of claim 9, wherein the gate insulating layer is comprised of silicon nitride.

13. The active matrix liquid crystal device of claim 9, wherein the passivation layer is comprised of silicon oxynitride formed at a temperature of about 200°C.